REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

Drawings

Applicant respectfully requests that the Examiner accept the formal drawings submitted on March 24, 2004.

Disposition of Claims

Claims 1-13 were pending in this application. By way of this reply, new claim 14 has been added. Accordingly, claims 1-14 are now pending in this application. Claims 1, 7, 9, and 13 are independent. The remaining claims depend, directly or indirectly, from claims 1, 7, 9, and 13.

New Claims

By way of this reply, new claim 14 has been added to recite that a noise error is caused by at least one selected from a ground glitch, a power glitch, and a high resistance path. No new subject matter has been added by way of new claim 14, as support for new claim 14 may be found, for example, on page 1, line 10 – page 2, line 3 and on page 9, lines 9-16 of the Specification.

Rejection(s) under 35 U.S.C. § 103

Claims 1-7 and 9-13 are rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,791,370 issued to Morzano (hereinafter "Morzano") in view of U.S. Patent

No. 5,729,208 issued to Ogiwara (hereinafter "Ogiwara"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a method and apparatus for detecting a noise error of a signal. As seen with respect to one or more embodiments of the invention, a self-diagnostic circuit (50) comprises comparators (58, 60), flip-flops (62a, 62b, 62c, 62d), and logic gates (64a, 64b, 66) (*see, e.g.*, Specification, Figure 2).

Transitions from high to low may be measured by flip-flops (62a, 62b), delay buffer (68a), and XOR gate (64a), while transitions from low to high may be measured by flip-flops (62c, 62d), delay buffer (68b), and XOR gate (64b) (*see e.g.,* Specification, page 5, line 18 – page 6, line 8). When there is a noise error in circuit (50), *i.e.*, when a signal other than a normal signal transition occurs, resulting from factors such as noise, a high-resistance path, etc., the logic of circuit (50) indicates an error at alarm output (70) (*see, e.g.*, Specification, page 6, lines 9-16).

Accordingly, independent claims 1 and 7 require a high comparator that references a high voltage limit with the signal and generates an output, and a low comparator that references a low voltage limit with the signal and generates an output, where an alarm is generated if a noise error is detected. Similarly, claim 9 requires comparing a high signal voltage with a high voltage limit and generating a first signal dependent thereon, activating an alarm if the high signal voltage is less than the high voltage limit. Claim 9 further requires comparing a low signal voltage with a low voltage limit and generating a second signal dependent thereon, and activating an alarm if the low signal voltage is greater than the low voltage limit. Claim 13 contains limitations similar to claim 9.

Morzano, in contrast to the present invention and as acknowledged by the Examiner, does not show or suggest that an alarm is generated if a noise error is detected.

Further, in clear contrast to the Examiner's assertions, Morzano completely fails to disclose a high comparator that references a high voltage limit with the signal and generates an output and a low comparator that references a low voltage limit with the signal and generates an output.

Morzano discloses a circuit for adjusting the clock skew of a differential clock signal (*see* Morzano, abstract). In contrast to the claimed invention, Morzano discloses a clock signal (100) and an inverse clock signal (101) input to respective input buffers (10, 11). As clearly seen in Figures 6a-6d of Morzano, V_{REF} is a single, constant signal used to compare transitions of clock signal (100) and inverse clock signal (101). In other words, V_{REF} detects which of the clock and inverse clock signals transition first (*see* Morzano, Figures 6a-6d, col. 6, line 62 – col. 7, line 19). It would be clear to one skilled in the art that Morzano does not disclose a high comparator and a low comparator as required by the claimed invention.

Ogiwara, like Morzano, does not show or suggest the above limitations of the claimed invention. This is evidenced by the fact that Ogiwara is used by the Examiner merely to show that an alarm is generated (*see* Office Action dated January 10, 2006, at page 3). Like Morzano, Ogiwara clearly discloses a pair of comparators (26, 28) that reference the *same* voltage signal V_{REF} (*see* Ogiwara, Figure 1; col. 3, lines 14-17). Thus, it would be clear to one skilled in the art that Ogiwara does not disclose referencing both a high voltage limit and a low voltage limit with respect to a signal, and generating outputs thereupon.

Further, even assuming *arguendo* that Ogiwara discloses the above limitations as asserted by the Examiner, it would be clear to one skilled in the art that Ogiwara is directed to non-analogous subject matter. Ogiwara is directed to a circuit for detecting *an open circuit* in a *hard-disk drive* (*i.e.*, a condition of breakage at the point at which coil wires in a hard disk drive are connected to an integrated circuit (see Ogiwara, col. 1, lines 9-25, col. 2, line 64 – col. 3, line 21). It would be clear to one skilled in the art that Ogiwara does not disclose a circuit related to

detecting a *noise error* of a signal. Rather, Ogiwara discloses generating an output when such an open-circuit condition is detected (*see* Ogiwara, Abstract).

Further, Applicant notes that there is no motivation to combine the cited references. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. There must be a suggestion or motivation to combine the references *within the prior art references themselves*. In other words, regardless of whether prior art references can be combined, there must an indication within the prior art references expressing desirability to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). Further, the present application *cannot be used as a guide* in reconstructing elements of prior art references to render the claimed invention obvious. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

One skilled in the art would not be motivated by Morzano, which is completely silent with respect to detecting a noise error of a signal **and** to hard-drive circuitry, to incorporate the teachings of Ogiwara without the present application as a guide. The Examiner assumes that it would be obvious to one skilled in the art "to implement the teaching of Ogiwara into Morzano as to ... accurately detect faulty condition as taught by Ogiwara (*see* Office Action dated January 10, 2006, at page 3). However, Morzano, which is directed to adjusting a clock skew of a signal, clearly provides no motivation to implement an alarm feature. Thus, one skilled in the art would not be motivated by Morzano to incorporate the teaching of Ogiwara, which is directed to detecting an *open circuit* condition in a hard drive.

Further, Ogiwara is silent with respect to detecting a noise error of a signal, as required by the claimed invention, and to adjusting a clock skew of a signal, as taught by Morzano. One skilled in the art would not be motivated by Ogiwara, which is completely silent

with respect to these features, to incorporate the teachings of Morzano without the present application as a guide. Ogiwara is directed to detecting an open-circuit condition in a hard drive. Thus, there is no motivation to combine the cited references.

In view of the above, Morzano and Ogiwara, (i) are not properly combinable, and (ii) whether taken separately or in combination, fail to show or suggest the present invention as recited in independent claims 1, 7, 9, and 13. Thus, independent claims 1, 7, 9, and 13 are patentable over Morzano and Ogiwara. Claims 2-6, 10-12, and 14, directly or indirectly dependent from claims 1, 7, 9, and 13, are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 06145/003001; P4928).

Dated: April 5, 2006

Respectfully submitted,

By _____

Thomas K. Scherer
Registration No.: 45,079
OSHA · LIANG LLP
1221 McKinney St., Suite 2800
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)
Attorney for Applicant

143665_1